R22 Regulation *Subject code:4E6DC*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VI Semester Regular/Supplementary Examinations, April 2026

VLSI DESIGN

(ECE)

Maximum Marks: 60 Date:18.04.2026 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 10 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X1M=10 Marks)		Marks	CO	Bloom Tx
1.a)	Write down the equations for I_{ds} of an n-channel enhancement MOSFET operating in Non-saturated region and saturated region?	1M	1	II
b)	Write the differences between CMOS and Bi-CMOS technologies.	1M	1	II
c)	What are the different MOS layers?	1M	2	I
d)	What is the purpose of stick diagrams in VLSI design?	1M	2	II
e)	What are the effects of wiring capacitance in VLSI circuits?	1M	3	II
f)	Define pseudo-NMOS logic.	1M	3	I
g)	What is meant by pipelining in data path design?	1M	4	II
h)	What is a parity generator?	1M	4	I
i)	How is a PLA different from PAL?	1M	5	II
j)	What is a lookup table (LUT) in FPGA?	1M	5	I

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	Bloom Tx
2	a) Derive an equation for drain-current Id of an n-channel enhancement MOSFET operating in active region. b) Write the fabrication steps of PMOS transistor with neat diagram.	5M 5M	1	III
	OR			
3	a) Analyze the transfer characteristics of CMOS inverter. b) Write the fabrication steps of NMOS transistor with neat diagram.	5M 5M	1	IV
4	a) Illustrate the lambda-based design rules with neat sketches. b) Draw the layout diagram of 2 input NAND gate with neat sketches.	5M 5M	2	III
	OR			
5	a) Describe the impact of MOS circuit scaling. b) Draw the layout diagram of 2 input NOR gate with neat sketches.	5M 5M	2	IV
6	What are alternate gate circuit. Explain any two of the circuits.	10M	3	IV

	OR			
7	What are the sources of capacitance in MOS design. Explain in brief.	10M	3	IV
8	Explain the design and working of 4-bit ripple carry adder and 4-bit carry look-ahead adder with necessary equations and compare their performance in terms of delay.	10M	4	IV
	OR			
9	a) Design a one detector circuit and explain its working with a suitable example. b) There are 3 inputs and 3 outputs, thus we need 8x3 ROM block. $f = \sum m(0, 1, 7)$ $g = \sum m(0, 3, 6, 7)$ $h = \sum m(0, 1, 3, 5, 7)$	5M 5M	4	III
10	a) Explain the need for testing in VLSI systems. Discuss its impact on yield and reliability. b) Design and implement Half adder using PAL and explain the steps involved.	5M 5M	5	IV
	OR			
11	Explain the architecture of CPLD and its components such as microcells and interconnects.	10M	5	II

2